Zhewen Pan

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EDUCATION

University of Wisconsin-Madison From Sep 2022
Ph.D. Student in Computer Engineering. GPA: 3.94

· Department of Electrical and Computer Engineering
· Advisor: Joshua San Miguel
· Research interests: Novel Architectures and Systems

University of Wisconsin-Madison Sep 2020 - May 2022
Master of Science in Computer Engineering. GPA: 3.94

· Department of Electrical and Computer Engineering
· Advisor: Joshua San Miguel

Purdue University Aug 2016 - May 2020
Bachelor of Science in Electrical Engineering (Highest Distinction). GPA: 3.99

· Department of Electrical and Computer Engineering

PUBLICATIONS

Zhewen Pan, Joshua San Miguel, Di Wu. **Carat: Unlocking Value-Level Parallelism in GEMMs**. *ACM Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2024.

Di Wu, Jingjie Li, Zhewen Pan, Younghyun Kim, Joshua San Miguel. **uBrain: A Unary Brain Computer Interface**. *International Symposium on Computer Architecture (ISCA)*, 2022.

Zhewen Pan, Joshua San Miguel. **The XOR Cache: A Catalyst for Compression**. *ACM Student Research Competition (SRC) Co-located w/ MICRO*, 2023.

Zhewen Pan, Di Wu, Joshua San Miguel. **T-MAC: Temporal Multiplication with Accumulation**. *The 4th Young Architect Workshop (YArch) Co-located w/ ASPLOS*, 2022.

RESEARCH

XOR Cache: A Catalyst for Compression Madison, WI

· Exploiting synergy between reversible transformations and prior cache compression schemes to boost compression ratio.
· Modeling the purposed compression scheme and cache coherence protocol in gem5 Ruby.

🏆 the ACM SRC 2023 SIGMICRO gold medal and grand finals 2nd place

Carat: Unlocking Value-Level Parallelism in GEMMs Madison, WI

· Implemented scheduling for the purposed temporal computing architecture in our in-house performance modeling platform
· Evaluated hardware efficiency through event-based power/energy modeling framework.

🏆 Distinguished Artifact Award

Unary Computing Brain Computer Interface Madison, WI

· Designed and synthesized hardware modules and performed regression analysis on efficiency statistics

Scalable Deadlock-Freedom Network-on-Chip Madison, WI

· Characterized deadlock criticality based on impact of positive feedback loop between congestion and deadlock formation
· Proposed and evaluated a scalable subactive deadlock-removal scheme based on packet bypassing using gem5-Garnet

EMPLOYMENT

Arm Inc May 2021 - Aug 2021
System IP Interconnect Performance Modeling Intern *Austin, TX (Remote)*

· Designed Out-of-the-Box test suite for Coherent Mesh Interconnect performance modeling flow, covering topology, traffic profile, runtime options, system address map variations
· Performed ad-hoc testing on performance application user interface and provided feedback

PROJECTS

Implementation of MLP-aware Cache Replacement Policy Madison, WI

· Implemented the MLP-aware LIN cache replacement policy in gem5 simulator
· Simulated and evaluated performance on the SPEC2006 CPU benchmark suite compiled for the x86 ISA
· Performed sensitivity analysis w.r.t varying L2 cache configuration and level of reordering aggressiveness

Dual-Core Coherent MIPS Processor Datapath and Memory System Design West Lafayette, IN

· Designed a 5-stage pipelined datapath with forwarding, and a 2-layer dynamic adaptive branch predictor
· Developed a coherent cache hierarchy implementing a snooping-based protocol
· Implemented lock-based synchronization hardware support in the multicore system to enforce write atomicity
· Verified design in gate-level simulation and prototyped the synthesized design on Altera FPGA

RoboTar: a Machine that Plays Guitar West Lafayette, IN

· Programmed a microcontroller to control servos and electromagnets to pluck and press the guitar strings
· Configured a Bluetooth BLE module to transfer ASCII encoded guitar tabs input to the system
· Designed, soldered and debugged PCBs for power circuit, current driving circuits, and microcontroller peripherals
· Created mechanical structure of the robot and incorporated the software and hardware systems

Bike Spokes Persistence of Vision Display West Lafayette, IN

· Programmed a Cortex M0 microcontroller to drive Neon Pixel LED strips
· Configured a Hall-effect sensor to generate interrupts to align the speed of the transfer with rotation
· Designed printed circuit board, power supply circuit and product packaging

AWARDS AND HONORS

Wisconsin Distinguished Graduate Fellowship - Schneider	2022-2023
ISCA Student Travel Grant	2022
gem5 Boot Camp Travel Grant	2022
Gold Medal in the ACM SIGMICRO Student Research Competition (SRC) Grad Division	2023
Distinguished Artifact Award (Carat)	2024
Department of ECE Gerald Holdridge Teaching Excellence Award	2024
Second Place in the ACM Student Research Competition (SRC) Grand Finals Grad Division	2023

PROFESSIONAL SERVICE

MICRO Artifact Evaluation Program Committee	2022
ISCA Undergrad Architecture Workshop (uArch) Mentor	2023

TEACHING

ECE552: Introduction to Computer Architecture	Fall 2023, Spring 2024
ECE554: Digital Engineering Laboratory	Spring 2022
ECE270: Digital System Design	Spring 2020
ECE362: Microprocessor Systems and Interfacing	Spring 2019
ECE270: Digital System Design	Spring 2018
ENGR131: Transforming Ideas to Innovation I	Fall 2017

SKILLS

Programming Languages	C, C++, Python, SystemVerilog, Verilog
Tools	gem5, Quartus, Modelsim, Altium, OpenRoad
Languages	Chinese (native), English (fluent), Japanese (beginner)